Innoscience 英诺赛科

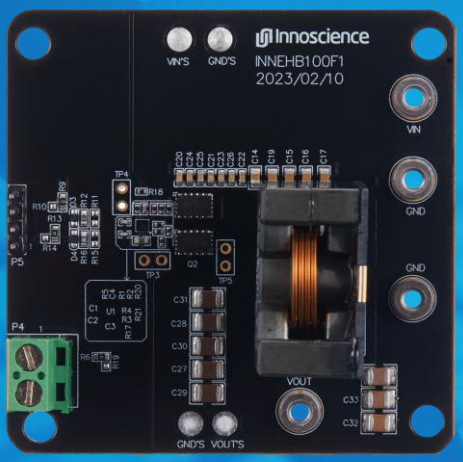
POWER THE FUTURE

INNEHB100F1

Evaluation Board Manual

100V GaN HEMT INN100FQ025A

Open Loop Half-Bridge EVB



CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by

ELECTRICAL SHOCK HAZARD

There may be a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

Contents

1. Overview

1.1. Introduction

INNEHB100F1 is a half-bridge evaluation board equipped with the half-bridge gate driver to evaluate the performance of 100V GaN HEMT INN100FQ025A. This board can simplify the test process, it can easily realize Buck converter with single or dual PWM input. The evaluation board can be used in BUCK circuit frequency range of 250kHz to 450kHz, input voltage range of 36V to 80V, under the frequency of 350kHz and the wind speed of 1400LFM, 48V-12V full load 30A efficiency can reach 97.10%. The board can be used not only for BUCK circuits, but also for BOOST circuits. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement and efficiency evaluation.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope（≥500MHz Bandwidth）
2) Two Low voltage DC power supply
3) PWM generator
4) Digital Multimeter
5) DC load (E-load or Power Resistor)

2. Performance Summary

The electrical characteristics of INNEHB100F1 are shown in **Table 1**.

Table 1 Electrical Characteristic (T_A=25℃)

Symbol	Parameters	Min	Typ	Max	Units
V_{DD}	V_{DD} supply Voltage	7	8	12	V
V_{IN}	Input Voltage	36	48	80(1)	V
F_{SW}	Switching frequency		350		kHz
P_{OUT}	Output Power			389(2)	W
EFF	Typical efficiency		97.10%(3)		
V_{PWM}	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		1.5	V

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100V for INN100FQ025A.

(2) Maximum output power with be subject to switching frequency, bus voltage, load current EVB temperature and thermal cooling.

(3) 97.10% is the efficiency at 48V to 12V, load 30A, frequency 350kHz, and the wind speed of 1400LFM.

3. Block Diagram

The system block diagram of INNEHB100F1 is shown in **Figure 1**.

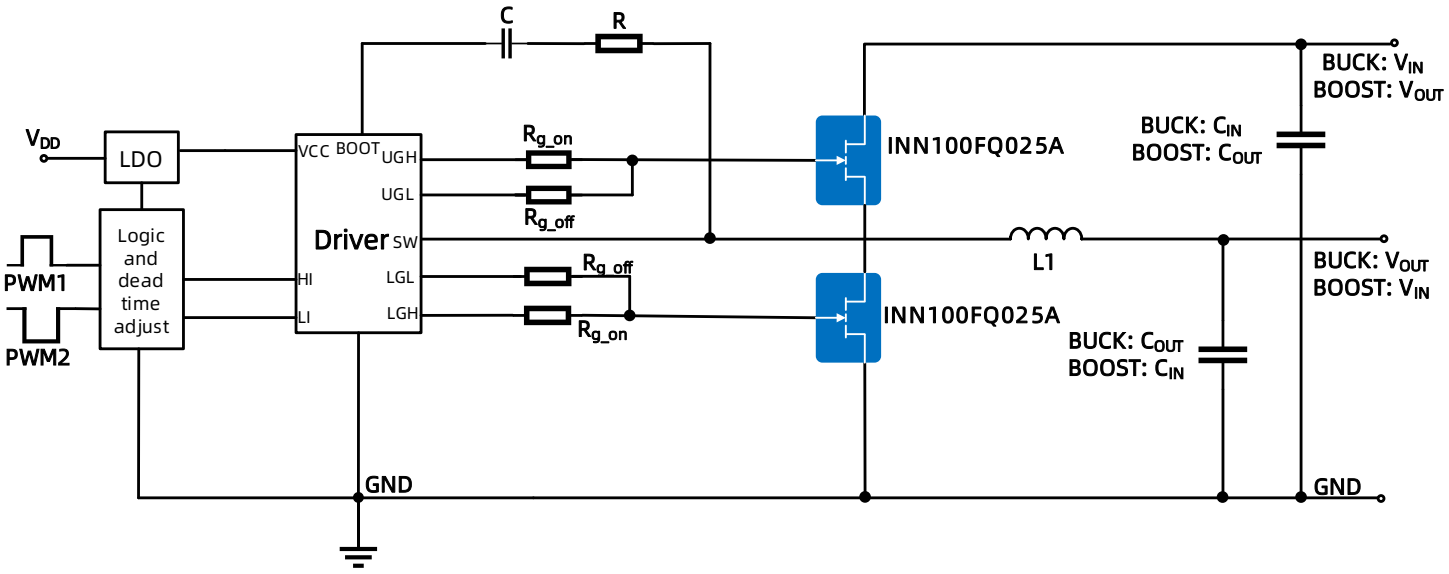


Figure 1 INNEHB100F1 Block Diagram

4. EVB Overview

The top and bottom views of the INNEHB100F1 board are shown in **Figure 2** and **Figure 3**.

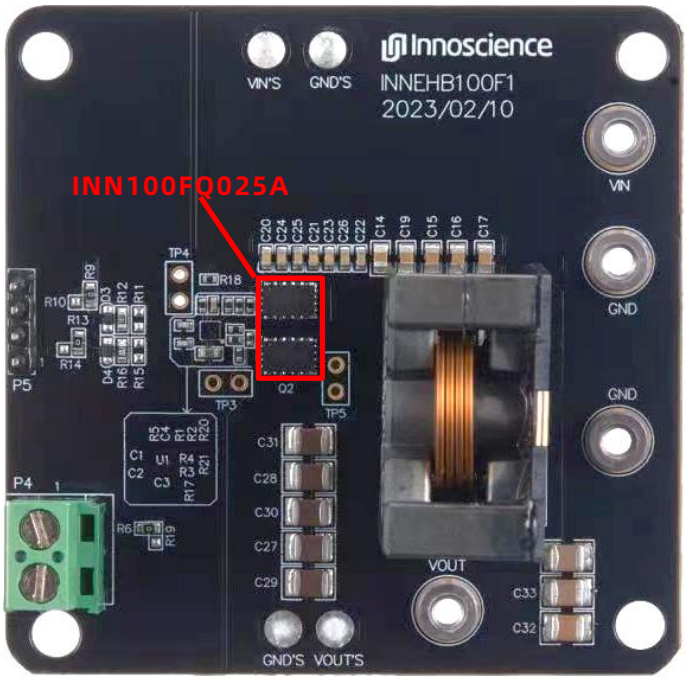


Figure 2 Top view of INNEHB100F1

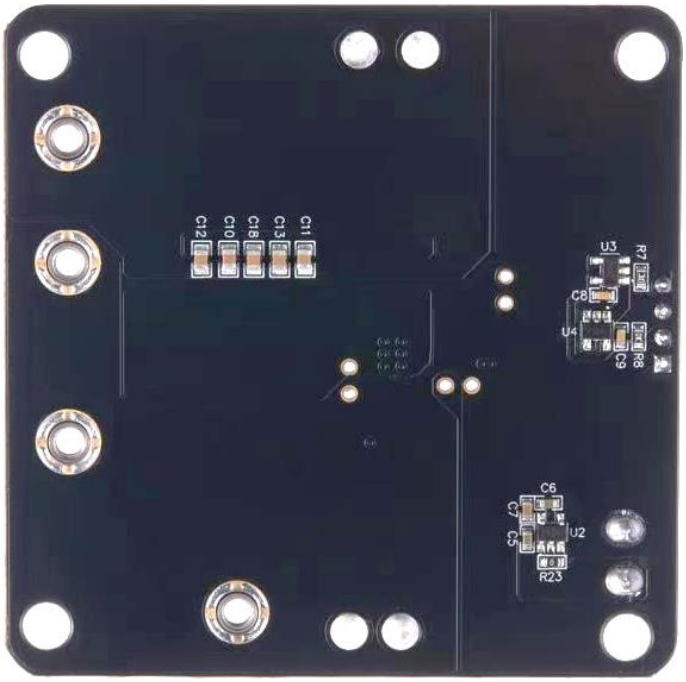
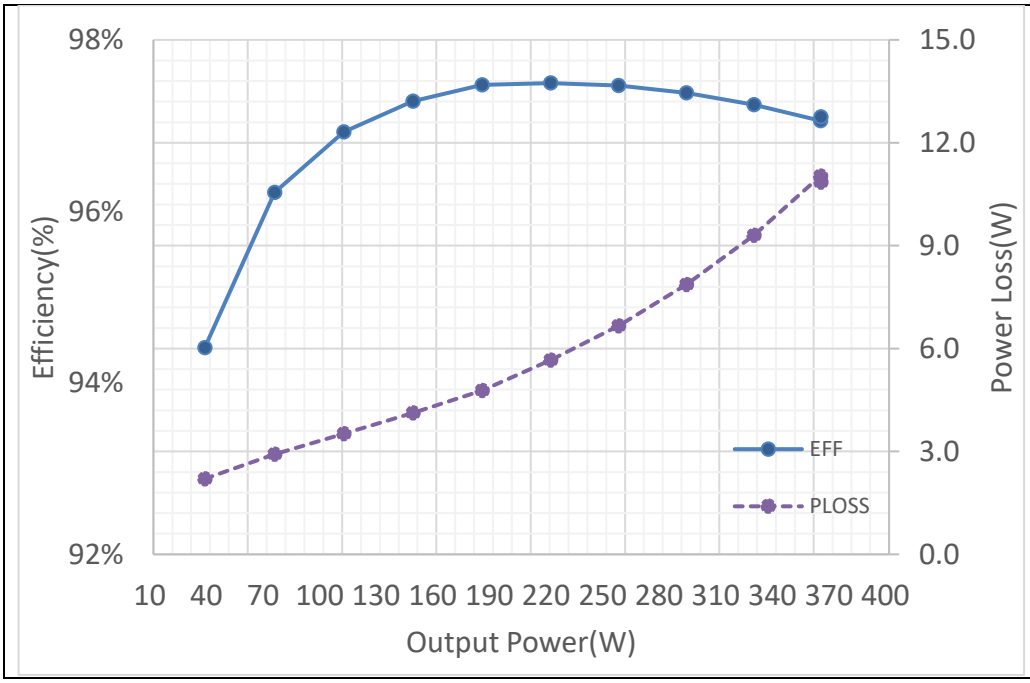


Figure 3 Bottom view of INNEHB100F1

5. Evaluation Results

5.1. Efficiency Results



Test conditions

Buck Mode

V_{IN}=48Vdc

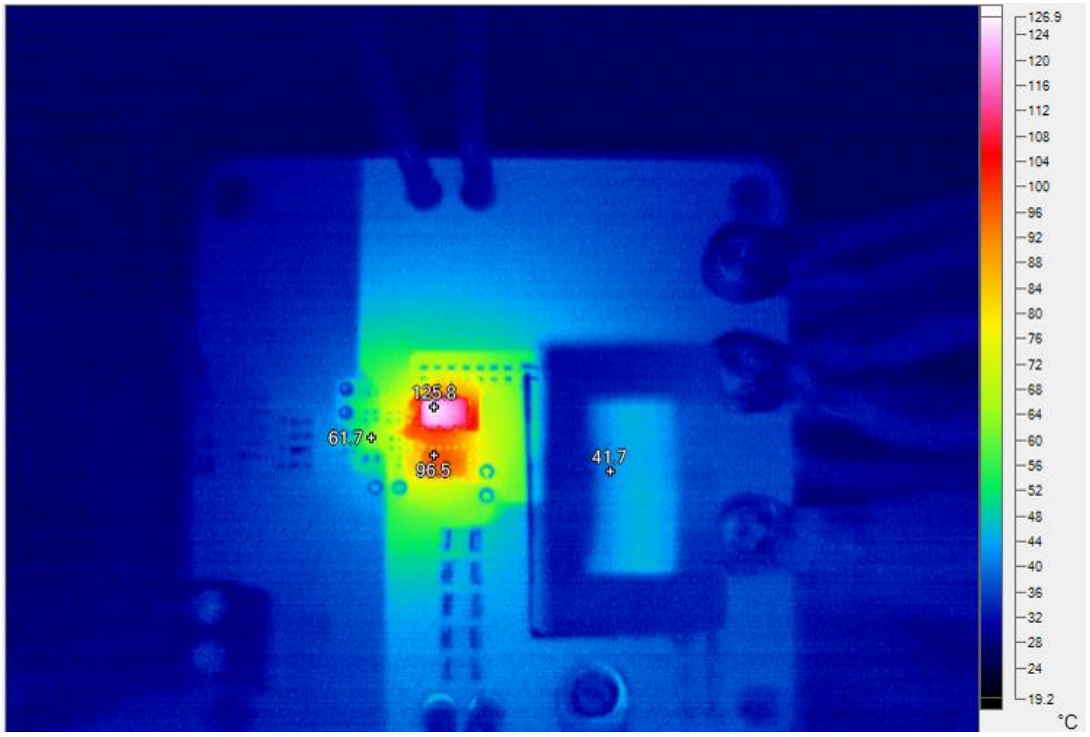
V_{OUT}=12Vdc

L=2.2uH

F_{SW}=350kHz

Airflow=1400LFM

5.2. Thermal performance



Test conditions

Buck Mode

V_{IN}=48Vdc

V_{OUT}=12Vdc

I_{OUT}=30A

L=2.2uH

f_{SW}=350kHz

Airflow=1400LFM

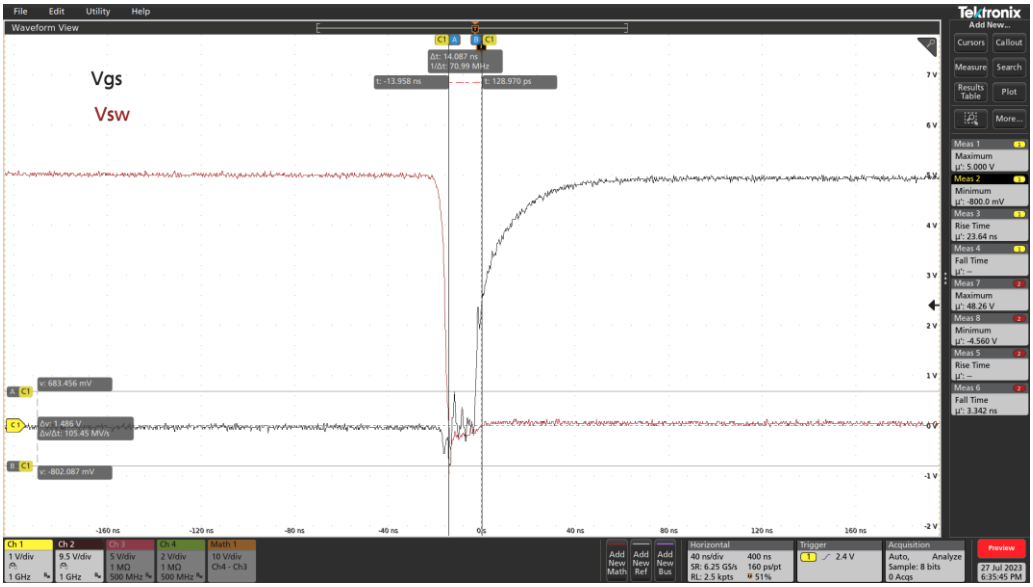
Result

Switching GaN : 125.8℃

Continuation GaN : 96.5℃

Inductor: 41.7℃

5.3. Switching Waveforms



Test conditions

Buck Mode

V_{IN}=48Vdc

V_{OUT}=12Vdc

I_{OUT}=30A

f_{SW}=350kHz

Airflow=1400LFM

R_{g_on}=3Ω, R_{g_off}=0Ω

Result

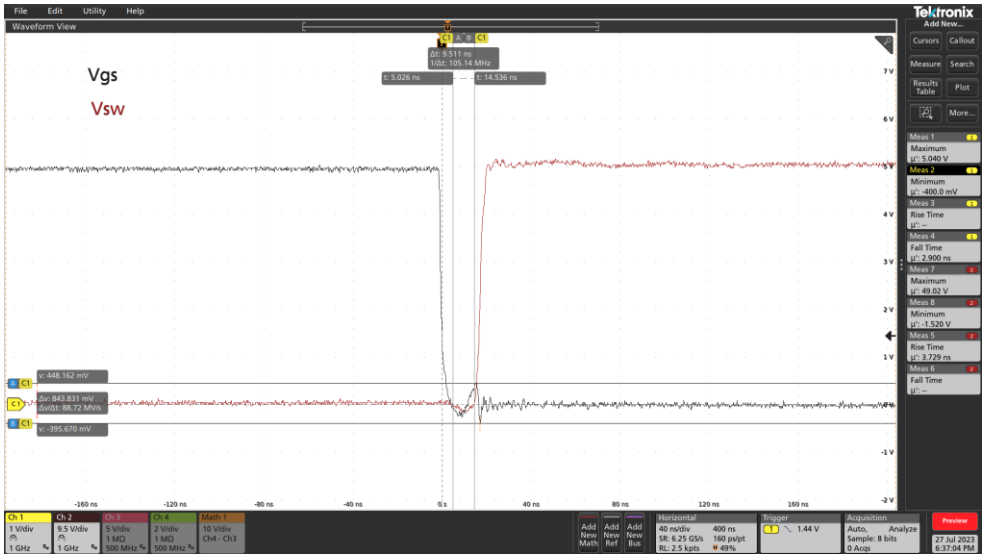
SW Edge:

Falling time=3.342ns

Falling Overshoot=-4.560V

LG Edge:

Rising time=23.64ns,



Test conditions

Buck Mode

V_{IN}=48Vdc

V_{OUT}=12Vdc

I_{OUT}=30A

f_{SW}=350kHz

Airflow=1400LFM

R_{g_on}=3Ω, R_{g_off}=0Ω

Result

SW Edge:

Rising Overshoot=1.02V

Rising time=3.729ns

LG Edge:

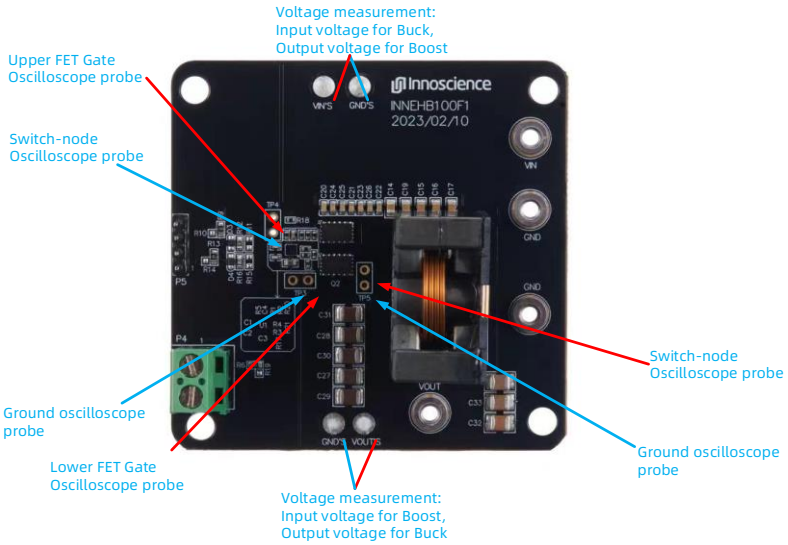
Falling time=2.900ns

Appendix

Appendix A. Testing guidance

1、 Test point location

The test points of INNEHB100F1 are shown in **Appendix Figure 1**.

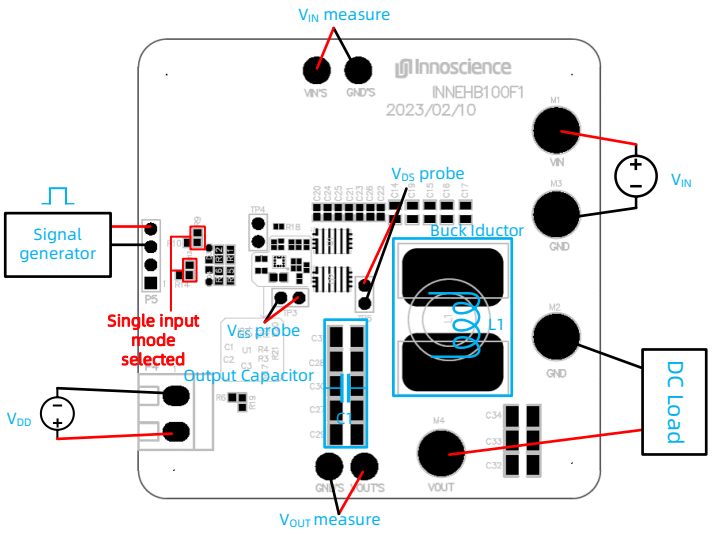


Appendix Figure 1 Measurement points

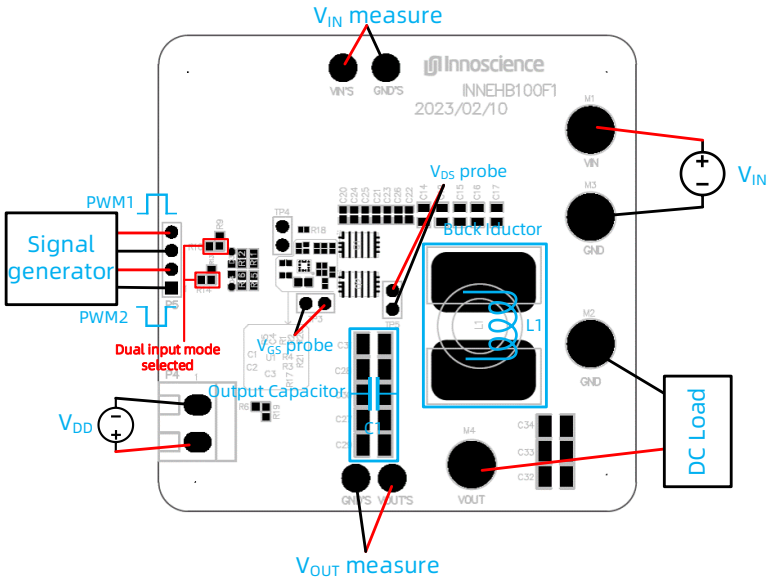
2、 Test setup

3.1 Buck Mode

In Buck mode, the wiring diagrams of INNEHB100F1 with single PWM input and dual PWM input are shown in **Appendix Figure 2** and **Appendix Figure 3**, respectively.



Appendix Figure 2 Single-PWM input Buck mode



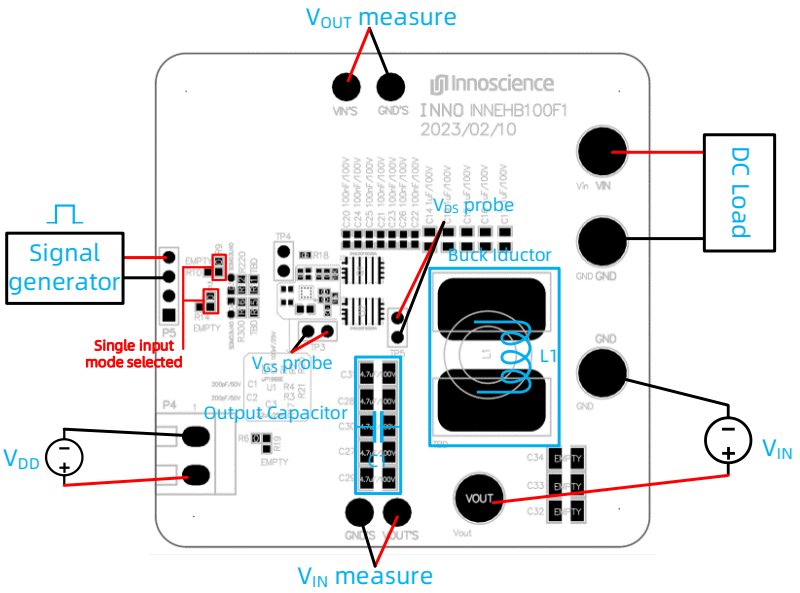
Appendix Figure 3 Dual-PWM input Buck mode

Before tests, single or dual PWM input modes could be selected. When selecting the single PWM input mode, please solder 0Ω resistor to R9 & R13. The dead time is regulated by R12, R16, C1 and C2. The value for R12 is 180Ω, and R16 is 360Ω. The value of C1 and C2 is 200 pF. At this time, at the load of 20A, the corresponding measured dead time between lower FET shutdown and upper FET opening is about 10ns, and the dead time between upper FET shutdown and lower FET opening is also about 10ns.

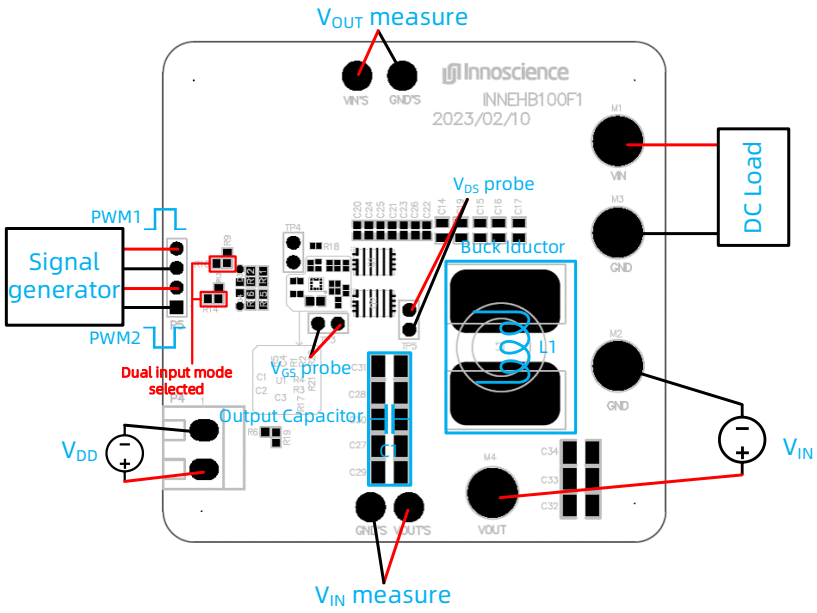
To select dual PWM mode, please solder 0Ω resistor to R10, R14, R12 and R16.Appendix Figure 3 shows the required PWM signals; PWM1 and PWM2 should be complementary. The dead time is controlled by the signal generator.

3.2 Boost Mode

In Boost mode, the wiring diagrams of INNEHB100F1 with single PWM input and dual PWM input are shown in Appendix Figure 4 and Appendix Figure 5, respectively.



Appendix Figure 4 Single-PWM input Boost mode



Appendix Figure 5 Dual-PWM input Boost mode

3、 Power up and down sequence

3.1 Power-up sequence (Buck Mode)

1) Check every power supply is **off.**

2) Connect the DC voltage source to **V_{IN}** terminal and common ground **GND** terminal, as shown in **Appendix Figure 2**(Pay attention to the polarity).

3) Connect the electronic load to pin **V_{OUT}.**

4) Connect the auxiliary source to the V_{DD} terminal **P4** (Pay attention to the polarity).

5) Connect the signal generator to pin **P5**.

6) Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.

7) Open the signal generator and enter the PWM signal with the required duty ratio and frequency.

8) Make sure the initial input supply voltage is 0V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.

9) Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

3.2 Power-up sequence (Boost Mode)

1) Check every power supply is **off**

2) Connect the DC voltage source to pin V_{OUT}, as shown in Appendix Figure 4 (Pay attention to the polarity).

3) Connect the positive pole of the electronic load to pin V_{IN} and the negative pole to pin **GND**.

4) Connect the auxiliary source to the V_{DD} terminal **P4** (Pay attention to the polarity).

5) Connect the signal generator to pin **P5**.

6) Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.

7) Open the signal generator and enter the PWM signal with the required duty ratio and frequency.

8) Make sure the initial input supply voltage is 0V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.

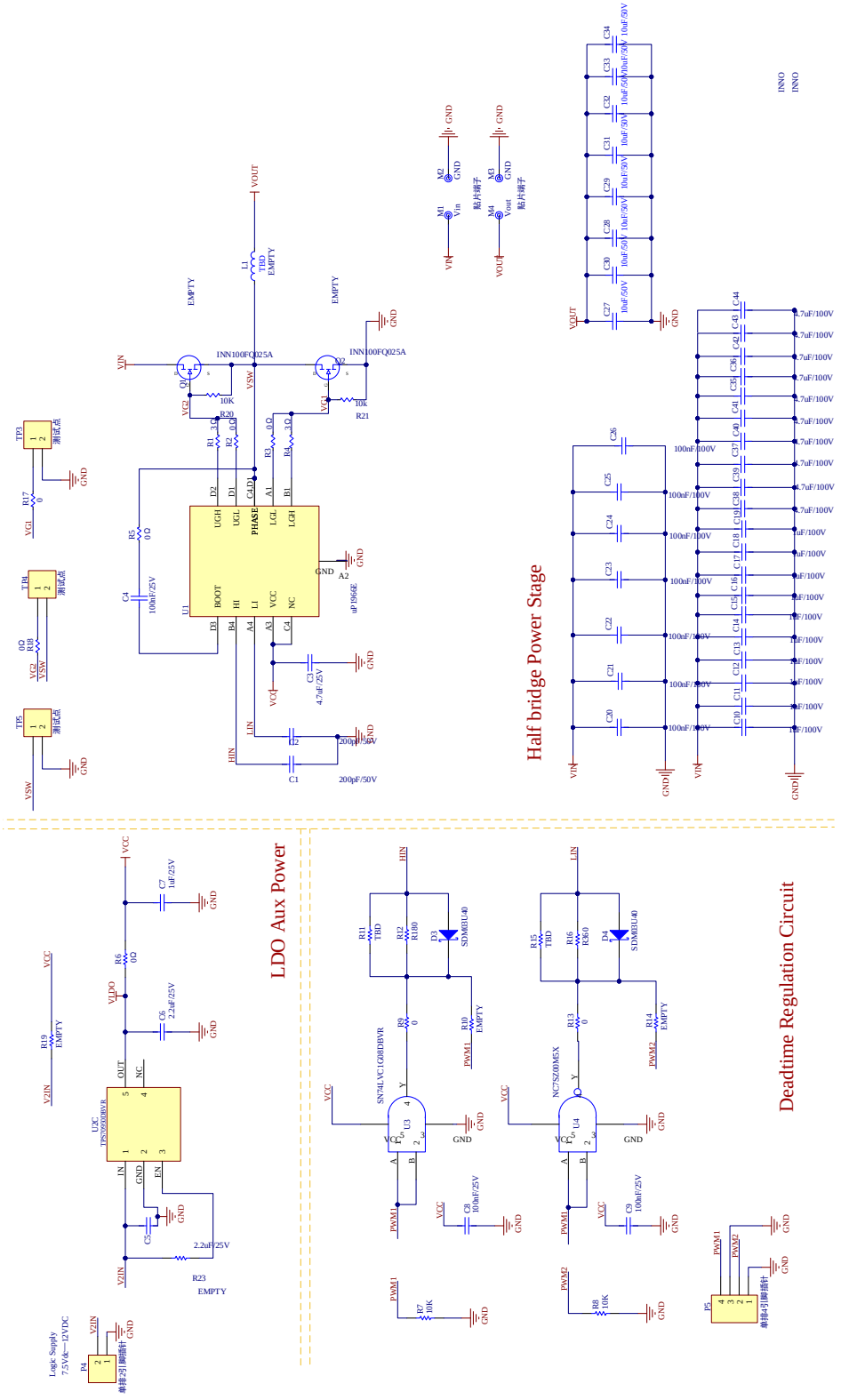
9) Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

3.3 Power-down sequence

1) Turn off the **E-load** first
2) Turn off the **DC voltage source**
3) Turn off the **PWM generator**
4) Turn off the **auxiliary power supply**

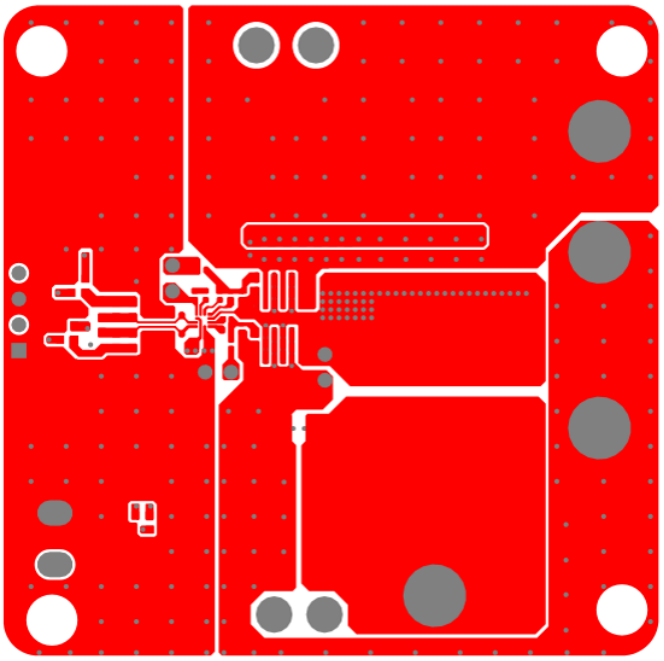
Appendix B. Schematic

The schematic diagram of INNEHB100F1 is shown in **Appendix Figure 6**.

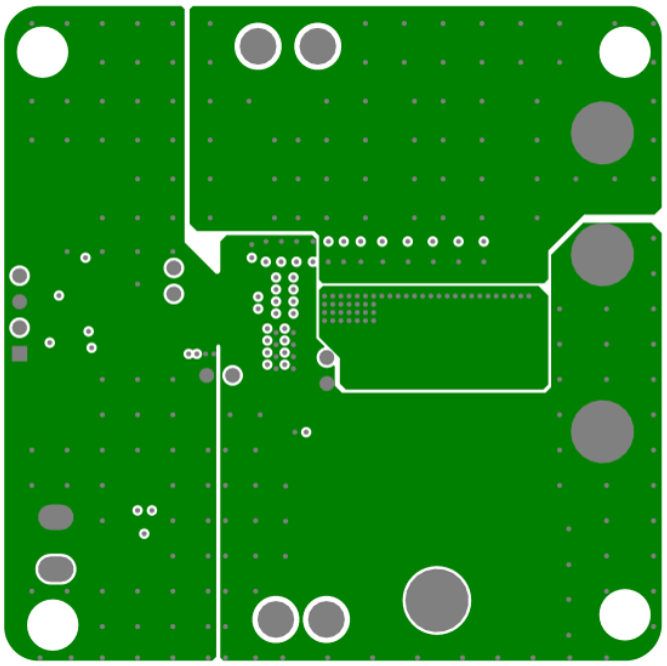


Appendix Figure 6 Schematic of INNEHB100F1

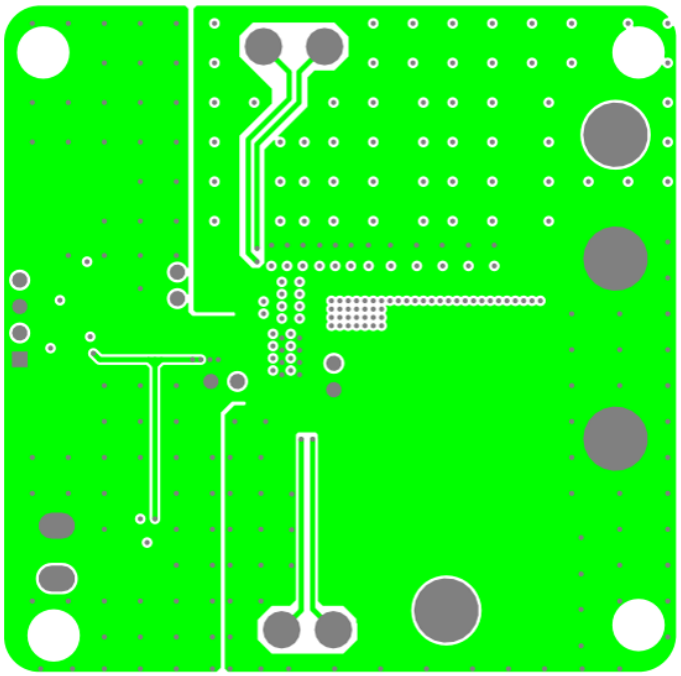
Appendix C. PCB Layout



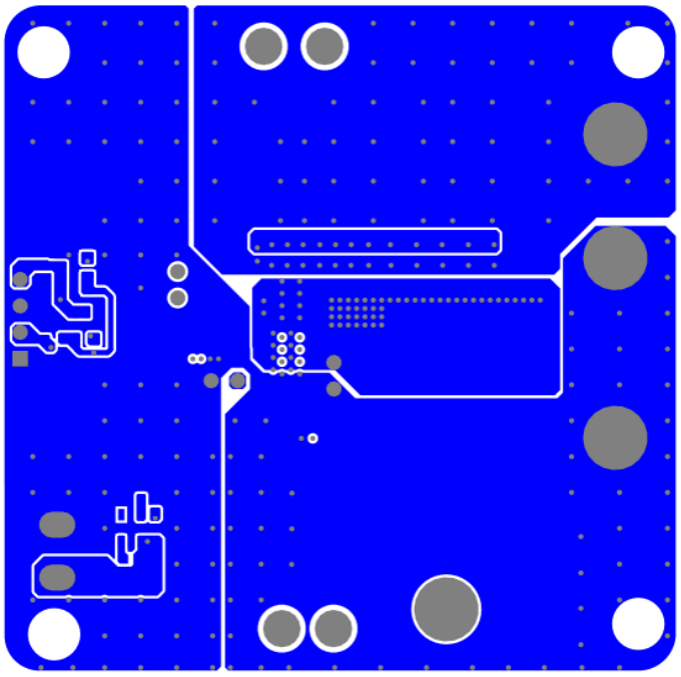
Appendix Figure 7 The top layer of INNEHB100F1



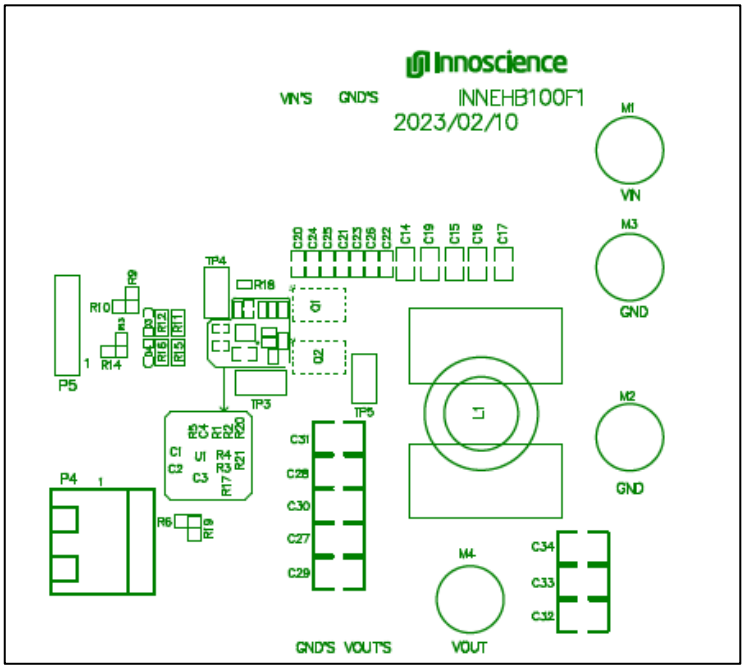
Appendix Figure 8 The first middle layer of INNEHB100F1



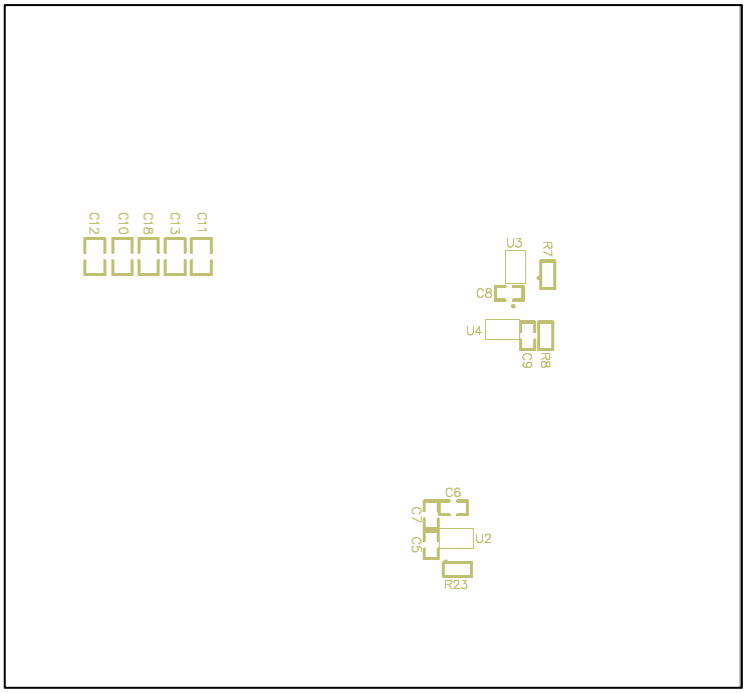
Appendix Figure 9 The second middle layer of INNEHB100F1



Appendix Figure 10 The bottom layer of INNEHB100F1



Appendix Figure 11 The top overlay of INNEHB100F1



Appendix Figure 12 The bottom overlay of INNEHB100F1

Appendix D. BOM

Designator	Part Number	Manufacturer	Description	Quantity
C1, C2	CC0402JRNPO9BN201	YAGEO	Cap,200pF,COG,50V	2
C5, C6	GRM188R61E225KA12D	MURATA	Cap,2.2uF,X5R,25V,±10%	2
C3	CL10A475KP8NNNC	SAMSUNG	Cap,4.7uF,X5R,25V,±10%	1
C4	0402B104K250CT	WALSIN	Cap,100nF,X7R,25V,±10%	1
C7	CL10B105KA8NNNC	SAMSUNG	Cap,1uF,X7R,25V,±10%	1
C8, C9	CL10B104KB8NNNC	SAMSUNG	Cap,100nF,X7R,50V,±10%	2
C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	HMK212BC7105KGHTE	TAIYO YUDEN	Cap,1uF,100V,±10%	10
C20, C21, C22, C23, C24, C25, C26	CL10B104KC8NNNC	SAMSUNG	Cap,100nF,X7R,100V,±10%	7
C27, C28, C29, C30, C31, C32, C33, C34	CL32B106KBJNNNE	SAMSUNG	Cap,10uF,X7R,50V,±10%	8
C35, C36, C37, C38, C39, C40, C41, C42, C43, C44	GRM32EC72A106KE05L	MURATA	Cap,4.7uF,100V,±10%	7
R2, R3, R5, R17, R18	RTT0200000FTH	RALEC	Res,0R,±1%, 0.1W,0402	5
R1, R4	RC-02U2R20FT	FH	Res,2.2R,±1%, 0.625W,0402	2
R6,R9,R13	0603WAF0000T5E	UNI-ROYAL	Res,0R,±1%, 0.1W,0603	3
R7, R8	0603WAF1002T5E	UNI-ROYAL	Res,10K,±1%, 0.1W,0603	2
R10, R11, R14, R15, R19, R23	EMPTY		Res	6
R12	0603WAF3000T5E	UNI-ROYAL	Res,180R,±1%, 0.1W,0603	1
R16	RS-03K5100FT	FH	Res,360R,±1%, 0.1W,0603	1
R20, R21	0402WGF1002TCE	UNI-ROYAL	Res,10K,±1%, 0.063W,0402	2
D3, D4	SDM03U40	DIODES	Schottky Diode，30V，0.3A，	2
L1	EMPTY		Inductance	1
Q1, Q2	INN100FQ025A	INNOSCIENCE	GAN FETs，100V/2.5mΩ，	2
U1	uP1966E	UPI SEMICONDUCTOR	Dual-Channel Gate Driver	1
U2	TPS70950DBVR-TP	TECH PUBLIC	LDO voltage regulators , fixed 5V output,	1
U3	SN74LVC1G08DBVR	TEXAS INSTRUMENTS	Single 2-Input Positive-AND Gate	1
U4	NC7SZ00M5X	ONSEMI	Two-Input NAND Gate	1

Revision History

Date	Versions	Description	Author
2023-09-08	1.0	First edition	AE Team
2025-03-07	1.1	Format modification, content optimization	AE Team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

Disclaimer:
Innoscience reserves the right to make changes to the products or specifications described in this document at any time. All information in this document, including descriptions of product features and performance, is subject to change without notice. INNOIC ACCEPTSURBIT ACCEPTS NO LIABILITY ARISING OUT OF THE USE OF ANY EQUIPMENT OR CIRCUIT DESCRIBED HEREIN. The performance specifications and operating parameters of the products described in this article are determined in a stand-alone state and are not guaranteed to be performed in the same manner when installed in the customer's product. Samples are not suitable for extreme environmental conditions. We make no representations or warranties, express or implied, as to the accuracy or completeness of the statements, technical information and advice contained herein and expressly disclaim any liability for any direct or indirect loss or damage suffered by any person as a result thereof. This document serves as a guide only and does not convey any license under the intellectual property rights of Innoscience or any third party.